Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

What is claimed is:

Claim 1. (original) Method for parallel production of a MOS transistor in an MOS area of a substrate and a bipolar transistor in a bipolar area of the substrate, comprising:

a) generating a MOS preparation structure in the MOS area, wherein the MOS preparation structure comprises an area provided for a channel, a gate dielectric, a gate electrode layer and a mask layer on the gate electrode layer;

b) generating a bipolar preparation structure in the bipolar area, wherein the bipolar preparation structure comprises a conductive layer and a mask layer on the conductive layer;

c) common structuring of the gate electrode layer and the conductive layer by using the mask layers for defining a gate electrode in the MOS area and a base terminal area and/or emitter collector terminal area in the bipolar area;

d) thinning the mask layer in the area of the gate electrode, so that a thinned mask layer remains in the area of the gate electrode; and

e) doping the conductive layer in the area of the gate electrode across the thinned mask layer.

Claim 2. (original) Method according the claim 1, wherein the mask layer has a first and a second isolation layer.

Claim 3. (original) Method according the claim 2, wherein in step d) a selective etching of the second isolation layer is performed down to the first isolation layer.

Claim 4. (original) Method according to claim 1, wherein the mask layer in the MOS area and the mask layer in the bipolar area is generated by common depositing of at least one isolation layer.

Claim 5. (original) Method according the claim 4, which further comprises the step of structuring the mask layer in the MOS area for defining the gate electrode and in the bipolar area for defining the base terminal area and/or collector area.

Claim 6. (original) Method according to claim 1, further comprising a step of common depositing of the conductive layer in the bipolar area and at least part of the gate electrode layer in the MOS area.

Claim 7. (original) Method according to claim 6, wherein the gate electrode layer has a first and a second gate electrode part layer, wherein the second gate electrode part layer is deposited in the bipolar area together with the conducive layer.

Claim 8. (original) Method according to claim 1, wherein prior to the common structuring a thinning of the gate electrode layer is performed.

Claim 9. (original) Method according to claim 1, wherein the step d) in the bipolar area a base terminal area and a window disposed therein for doping a collector area and/or a base area are structured from the conductive layer.

Claim 10. (original) Method according to claim 1, wherein in step d) in the bipolar area, a collector terminal area and an emitter terminal area are structured from the conductive layer.

Claim 11. (original) Method according to claim 1, wherein on the mask layer an antireflection layer is generated.

Claim 12. (original) Method according to claim 1, further comprising, after step d), doping of a collector area and/or a base area in the bipolar area, and a common doping of a source area and/or drain area in the channel area and the gate electrode.

Claim 13. (original) Method according claim 1, wherein step d) further comprises simultaneous etching of the gate electrode layer and conductive layer.

Claim 14. (original) Method according to claim 1, further comprising a step of simultaneously generating isolating spacing layers on side walls of the gate electrode layer in

the MOS area and the conductive layer in the bipolar area, wherein the isolating spacing layers in the MOS area serve for the definition of areas to be doped in the MOS area and for the isolation of a base area and an emitter area in the bipolar area.

Claim 15. (original) Method according to claim 14, wherein the step of simultaneously generating spacing layers comprises applying first and second spacing layers and a selective etching of the first spacing layer and the second spacing layer.

Claim 16. (original) Method according to claim 1, further comprising a parallel generation of one or several devices of the group, which comprises a varactor diode and a MOS capacitor.

Claims 17-20. (canceled)